STIC Fast & Focused search results for case #10/719814
May 18,2006

BIBLIOGRAPHIC PATENTS

File 347:JAPIO Dec 1976-2005/Dec(Updated 060404)
(c) 2006 JPO & JAPIO
File 350:Derwent WPIX 1963-2006/UD,UM &UP=200631
(c) 2006 Thomson Derwent

Set	Items	Description
S1	629674	CPU OR CENTRAL()PROCESS???()UNIT? ? OR PROCESSOR? ?
S2	22974	CACHE? ?
S3	10173	TEMPORARY(3N)(STORAGE OR MEMORY)
S4	841090	EXTERNAL(3N)(STORAGE OR MEMORY) OR DISK? ? OR DISC? ? OR H-ARD(2N)DRIVE? ? OR HARDDRIVE? ? OR HARDDISK? ? OR HARDDISC? ? OR HDD OR HD OR RAM OR RANDOM()ACCESS()MEMORY
S5	629	S4(3N)(INACCESSIBLE OR (NO OR .NOT. OR DOESNT OR DOESN()T - OR DONT OR DON()T OR WONT OR WON()T OR CANT OR CAN()T OR CANN-OT OR INHIBIT??? OR PROHIBIT??? OR STOP? ? OR STOPP???)(2N)(A-CCESS??? OR READ??? OR WRIT???))
S6	111784	POWER???(3N)(OFF OR DOWN OR STOP? ? OR STOPP??? OR (SHUT? ? OR SHUTTING OR TURN??? OR CUT OR CUTS OR CUTTING)(3N)(OFF OR DOWN) OR CONSERV???) OR STANDBY OR STAND()BY
S7	2	S1 AND S2:S3 AND S5 AND S6
S8	10	S1 AND S2:S3 AND S5
S9	8	S8 NOT S7
S10	8	S9 NOT AD=20031121:20060518/PR
S11	134	S1 AND S2:S3 AND S6
S12	1053	S4(3N)(DONT OR DON()T OR DOESNT OR DOESN()T OR "NOT" OR IS-NT OR ISN()T)(2N)(NEED??? OR USE OR USED OR USES OR USING)
S13	0	S12 AND S11
S14	111	S11 AND IC=G06F
S15	407	S2:S3(2N)(ONLY OR JUST OR SOLE?? OR ALONE)
S16	4	S15 AND S14
S17	4	S16 NOT (S7 OR S9)
S18	3	S17 NOT AD=20031121:20060518/PR
S19	81	S2:S3(5N)POWER(3N)(CONTROL? ? OR CONTROLL???)
S20	8	S14 AND S19
S21	8	S20 NOT (S7 OR S9 OR S17)
S22	8	S21 NOT AD=20031121:20060518/PR
S23	20	S12 AND S2:S3
S24	0	S23 AND (POWER??? OR STANDBY OR STAND()BY OR SLEEP)
S25	20	S23 NOT (S7 OR S9 OR S17 OR S21)
S26	20	S25 NOT AD=20031121:20060518/PR

7/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

03478130 **Image available**
OPTICAL DISK DEVICE

PUB. NO.: 03-141030 [JP 3141030 A]
PUBLISHED: June 17, 1991 (19910617)
INVENTOR(s): OKADA OSAMU
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-275974 [JP 89275974]
FILED: October 25, 1989 (19891025)
INTL CLASS: [5] G11B-007/00; G06F-003/06; G06F-003/06
JAPIO CLASS: 42.5 (ELECTRONICS -- Equipment); 45.3 (INFORMATION PROCESSING -- Input Output Units)
JAPIO KEYWORD:R002 (LASERS); R099 (ELECTRONIC MATERIALS -- Single Crystal Ferrite & Magnetic Bubble Element; R102 (APPLIED ELECTRONICS -- Video Disk Recorders, VDR)
JOURNAL: Section: P, Section No. 1251, Vol. 15, No. 363, Pg. 93, September 12, 1991 (19910912)

ABSTRACT

PURPOSE: To improve the reliability at the time of **cutting off** a **power** source by allowing a buffer memory to have a **power** source **cut - off** emergency processing function, and to decrease the power consumption by continuing only the rotation of a **disk** when there is **no access** request to an optical disk.

CONSTITUTION: When there is an access request, data is read out of an optical disk 2, it is rewritten and saved in a bubble memory being a buffer memory or a Bloch line memory, operated as a **cache** memory, and data write is trans ferred to the optical disk after writing it in the bubble memory or the Bloch line memory. A **power** source **cut - off** detector 6 detects **cut - off** at a line input point of a system power source, and by a **power** source **cut - off** emergency **processor** 7, **power** supply voltage of a short time to the bubble memory or the Bloch line memory is executed and a data loss is prevented, and when a new access to the optical disk is not requested, an optical head position is locked in a state that a rotation of the disk remains continued, a laser light emission is stopped, the reliability of the system is increased, and the power consumption is decreased.

[***** Your application *****]
7/5/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016290207 **Image available**
WPI Acc No: 2004-448102/200442
XRPX Acc No: N04-354422
CPU **of personal computer, forbids access to external memory such as dynamic RAM, if processing of task is possible only with access to** cache

Patent Assignee: SHARP KK (SHAF); KAMEI N (KAME-I); KINOSHITA H (KINO-I); MINAMI T (MINA-I); MIZUYAMA Y (MIZU-I); NISHIMURA M (NISH-I); YOSHIMURA S

(YOSH-I)
Inventor: KAMEI N; KINOSHITA H; MINAMI T; MIZUYAMA Y; NISHIMURA M; YOSHIMURA S
Number of Countries: 002 Number of Patents: 002
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 20040103253 A1 20040527 US 2003719814 A 20031121 200442 B
JP 2004178016 A 20040624 JP 2002340055 A 20021122 200442

Priority Applications (No Type Date): JP 2002340055 A 20021122
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20040103253 A1 20 G06F-012/00
JP 2004178016 A 26 G06F-012/08

Abstract (Basic): US 20040103253 A1

NOVELTY - A control unit determines whether processing of task is possible only based on access to **cache** , depending on the amount of memory space used for task processing. The control unit forbids access to external memory such as dynamic RAM, when processing of the task is possible.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) information **processor** ; and

(2) method for controlling **CPU** .

USE - **CPU** of information **processor** (claimed) e.g. personal computer (PC) connected to external memory such as dynamic RAM (DRAM), ROM.

ADVANTAGE - Improves processing speed by performing operation in **CPU** , without using external memory for task processing. Power consumption is reduced effectively, by **stopping** supply of **power** to **external memory**0 during **inhibited access** to the memory.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart explaining the operation of the **CPU** .

pp; 20 DwgNo 5a/7

Title Terms: **CPU** ; PERSON; COMPUTER; ACCESS; EXTERNAL; MEMORY; DYNAMIC; RAM; PROCESS; TASK; POSSIBILITY; ACCESS; **CACHE**
Derwent Class: T01
International Patent Class (Main): G06F-012/00; G06F-012/08
International Patent Class (Additional): G06F-001/26; G06F-001/32; G06F-009/30; G06F-012/12
File Segment: EPI

10/5/5 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015645080 **Image available**
WPI Acc No: 2003-707263/200367
XRPX Acc No: N03-564976

Direct memory access transmitter for host computers, has transmit state machine which inhibits **data** read **from** RAM **, when most recent copy of requested data is in local** cache **memory**

Patent Assignee: EMC CORP (EMCE-N)

Inventor: KALLAT A; THIBAULT R
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 6584513 B1 20030624 US 2000540827 A 20000331 200367 B

Priority Applications (No Type Date): US 2000540827 A 20000331
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 6584513 B1 40 G06F-013/00

Abstract (Basic): US 6584513 B1
NOVELTY - A **CPU** transmits a control signal indicating whether the data read from RAM is the most recent copy of requested data or whether the most recent copy is in local **cache** memory. If the most recent copy is in local **cache** memory, a transmit state machine inhibits the read data and sends another data transfer request at the same address, for the most recent copy of the requested data.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for method of performing direct memory access transfers of data.
USE - For performing direct memory access (DMA) transfers of data between RAM and host computers/servers.
ADVANTAGE - The time required for transfer of data is reduced, thus reduction in operating bandwidth of interface is prevented. The total system failure is prevented, during the event of failure in a component or subassembly of the storage system.
DESCRIPTION OF DRAWING(S) - The figures show the flowcharts explaining the operation of direct memory access transmitter.
pp; 40 DwgNo 14A, 14B/15
Title Terms: DIRECT; MEMORY; ACCESS; TRANSMIT; HOST; COMPUTER; TRANSMIT; STATE; MACHINE; INHIBIT; DATA; READ; RAM; RECENT; COPY; REQUEST; DATA; LOCAL; **CACHE** ; MEMORY
Derwent Class: T01
International Patent Class (Main): G06F-013/00
File Segment: EPI

10/5/6 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012887522 **Image available**
WPI Acc No: 2000-059356/200005
XRPX Acc No: N00-046581
Disc memory device e.g. HDD - has CPU which stops supply of driving electric power to reading circuit by electric-power controller during condition in which data in buffer area of buffer memory is not forwarded to host
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: ICHIKAWA Y; ISHII S; KAWASAKI M
Number of Countries: 002 Number of Patents: 002
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
JP 11317000 A 19991116 JP 98121140 A 19980430 200005 B

US 6332196 B1 20011218 US 99244421 A 19990204 200205

Priority Applications (No Type Date): JP 98121140 A 19980430
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
JP 11317000 A 20 G11B-019/00
US 6332196 B1 G06F-001/26
Abstract (Basic): JP 11317000 A

NOVELTY - A **CPU** stops the supply of the driving electric power to the reading circuit by the electric-power controller during a first condition in which data in the buffer area of the buffer memory is not forwarded to the host. DETAILED DESCRIPTION - A buffer controller detects the transition from the first condition to the second condition, in which an idle of a predetermined amount is produced in the buffer memory by the forwarding of data in the buffer area of the buffer memory to the host, and outputs a detecting signal. The **CPU** responds to the output and restarts the supply of the driving electric power to the reading circuit by the electric-power controller. The buffer area stores temporarily the data read from a disc (11). An INDEPENDENT CLAIM is included for an electric-power supply control procedure.

USE - None given.

ADVANTAGE - Reduces power consumption since the electric-power supply to circuit that participates in **disc access** operation is **stopped** until the detecting signal is output. DESCRIPTION OF DRAWING(S) - The figure shows an explanatory drawing of operation with a flowchart for explaining the operation after the point reading **cache** completion. (11) Disc.

Dwg.2/20

Title Terms: DISC; MEMORY; DEVICE; **CPU** ; STOP; SUPPLY; DRIVE; ELECTRIC; POWER; READ; CIRCUIT; ELECTRIC; POWER; CONTROL; CONDITION; DATA; BUFFER; AREA; BUFFER; MEMORY; FORWARDING; HOST
Derwent Class: T03; W04
International Patent Class (Main): G06F-001/26; G11B-019/00
International Patent Class (Additional): G06F-001/28; G06F-001/30
File Segment: EPI

[**** Your application****]
18/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

08065257 **Image available**
CPU , INFORMATION **PROCESSOR** HAVING IT, AND CONTROL METHOD FOR **CPU**

PUB. NO.: 2004-178016 [JP 2004178016 A]
PUBLISHED: June 24, 2004 (20040624)
INVENTOR(s): KAMEI NAOYUKI
YOSHIMURA SOICHI
NISHIMURA MICHIAKI
MIZUYAMA YOSHIO
KINOSHITA HIROKI
MINAMI TAKAHIRO
APPLICANT(s): SHARP CORP

APPL. NO.: 2002-340055 [JP 2002340055]
FILED: November 22, 2002 (20021122)
INTL CLASS: **G06F-012/08** ; **G06F-001/26** ; **G06F-001/32** ; **G06F-009/30** ; **G06F-012/12**

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **CPU** , an information **processor** having it, and a control method for it capable of quick processing by performing processing inside it without using any external memory and **stopping power** supply to the external memory for reduction in power consumption.

SOLUTION: The **CPU** 10 is provided with a bus interface 11, a control unit 12, a command **cache** 13a, a data **cache** 13b, a secondary **cache** 13c, a command decoder 14, a computing unit 15, and a register group 16. The **CPU** 10 forbids access to the external memory and **stops power** supply to the external memory if processing can be carried out **only** by the **caches** 13a-13c.

22/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06562842 **Image available**
POWER CONSUMPTION REDUCING DEVICE

PUB. NO.: 2000-148582 [JP 2000148582 A]
PUBLISHED: May 30, 2000 (20000530)
INVENTOR(s): FUKAZAWA SATOSHI
APPLICANT(s): NEC KOFU LTD
APPL. NO.: 10-324077 [JP 98324077]
FILED: November 13, 1998 (19981113)
INTL CLASS: **G06F-012/06** ; **G06F-012/00**

ABSTRACT

PROBLEM TO BE SOLVED: To reduce **power** consumption by controlling the **power down** mode by a **cache** hit so as to set up a **power down** mode for a long period.

SOLUTION: The power consumption reducing device has a memory access control circuit 3 for converting a memory access instruction issued from a **CPU** 1 into a memory access format of a storage device 6 to be an aggregate of plural synchronous dynamic random access memories(SDRAMs) and a mode switching control circuit 5 for detecting the memory access instruction hits or misses in a **cache** 4 built in a memory controller 2 and executing a **power down** mode or a memory access. Thus power consumption can be reduced by setting up the storage device 6 to the **power down** mode by the circuit 5.

22/5/7 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011385929 **Image available**
WPI Acc No: 1997-363836/199733
XRPX Acc No: N97-302432
Power management apparatus for memory controllers - in which target controller controls exchange of information between processor **and target circuit e.g. DRAM in accordance with sequencing signal**
Patent Assignee: INTEL CORP (ITLC)
Inventor: CHUNG C; KARDACH J P; ZILLER J; CHIH-HUNG C
Number of Countries: 075 Number of Patents: 013
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9724653	A1	19970710	WO 96US20807	A	19961227	199733 B
AU 9713559	A	19970728	AU 9713559	A	19961227	199746
US 5692202	A	19971125	US 95581164	A	19951229	199802
GB 2322212	A	19980819	WO 96US20807	A	19961227	199835
			GB 9812477	A	19980611	
DE 19681716	T	19981126	DE 196081716	A	19961227	199902
			WO 96US20807	A	19961227	
US 5884088	A	19990316	US 95581164	A	19951229	199918
			US 97893443	A	19970710	
CN 1214130	A	19990414	CN 96180156	A	19961227	199933
GB 2322212	B	20000614	WO 96US20807	A	19961227	200032
			GB 9812477	A	19980611	
KR 99076908	A	19991025	WO 96US20807	A	19961227	200052
			KR 98705036	A	19980629	
TW 394871	A	20000621	TW 97101648	A	19970213	200109
KR 329344	B	20020509	WO 96US20807	A	19961227	200272
			KR 98705036	A	19980629	
DE 19681716	B4	20040226	DE 196081716	A	19961227	200415
			WO 96US20807	A	19961227	
CN 1147773	C	20040428	CN 96180156	A	19961227	200610

Priority Applications (No Type Date): US 95581164 A 19951229; US 97893443 A 19970710
Cited Patents: US 5493684; US 5511205
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9724653	A1	E	24	G06F-001/32	

Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG US UZ VN
Designated States (Regional): AT BE CH DE DK EA ES FI FR GB GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG

AU 9713559	A	G06F-001/32	Based on patent WO 9724653
US 5692202	A	12 G06F-001/32	
GB 2322212	A	G06F-001/32	Based on patent WO 9724653
DE 19681716	T	G06F-013/00	Based on patent WO 9724653
US 5884088	A	G06F-001/32	Cont of application US 95581164
			Cont of patent US 5692202

CN 1214130 A G06F-001/32
GB 2322212 B G06F-001/32 Based on patent WO 9724653
KR 99076908 A G06F-001/32 Based on patent WO 9724653
TW 394871 A G06F-001/26
KR 329344 B G06F-001/32 Previous Publ. patent KR 99076908
Based on patent WO 9724653
DE 19681716 B4 G06F-001/32 Based on patent WO 9724653
CN 1147773 C G06F-001/32

Abstract (Basic): WO 9724653 A

The computer system monitors the activity of a bus controller (208) of a **processor** (204), and in response controls the power consumption of a target controller e.g. a memory controller (216) coupled to the bus controller (208). A bus activity monitor (212) generates a bus activity signal that indicates activity in the bus controller (208).

The target controller (memory controller (216)) controls the exchange of information between the **processor0** (204) and a target circuit e.g. a DRAM (218). The target controller (216) has an input (215) for receiving a sequencing signal. A power management circuit (220) controls the power consumption of the target controller (216), and receives the bus activity signal and generates the sequencing signal in response to the bus activity signal.

USE - **Power** management in computer systems e.g. memory **controllers** , **cache controllers** , static RAM etc., by reducing or **shutting off power** in times of idleness.

Dwg.2/6

Title Terms: POWER; MANAGEMENT; APPARATUS; MEMORY; CONTROL; TARGET; CONTROL ; CONTROL; EXCHANGE; INFORMATION; **PROCESSOR** ; TARGET; CIRCUIT; DRAM; ACCORD; SEQUENCE; SIGNAL

Derwent Class: T01

International Patent Class (Main): **G06F-001/26** ; **G06F-001/32** ; **G06F-013/00**

International Patent Class (Additional): **G06F-011/30**

File Segment: EPI

26/5/5 (Item 5 from file: 347)

DIALOG(R)File 347:JAPIO

03817655 **Image available**

SIMULATION SYSTEM FOR DISK **CACHE** DEVICE

PUB. NO.: 04-182755 [JP 4182755 A]

PUBLISHED: June 30, 1992 (19920630)

INVENTOR(s): NISHIOKA TORU
SAITO MASATOSHI

APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)

APPL. NO.: 02-312376 [JP 90312376]

FILED: November 16, 1990 (19901116)

INTL CLASS: [5] G06F-012/08; G06F-012/08

JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 42.5 (ELECTRONICS -- Equipment)

JOURNAL: Section: P, Section No. 1438, Vol. 16, No. 502, Pg. 158,

October 16, 1992 (19921016)

ABSTRACT

PURPOSE: To easily and accurately confirm whether it is effective or **not** to **use** a **disk cache** device by simulating the access operation of a processor for which the disk **cache** device 13 is connected by using this measured data 31.

CONSTITUTION: A measured data 31 on the condition of access to a disk device 12 is acquired when a disk **cache** device 13 is not connected and the access operation of above-mentioned processor 11 in a state where the disk **cache** device 13 is connected is simulated by using this measured data 31. According to the above, it is easily and accurately to confirm whether it is effective or **not** to **use** a **disk cache** device.

26/5/19 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007595418 **Image available**
WPI Acc No: 1988-229350/198833
XRPX Acc No: N88-174514
Data processing system operation with rotating storage access - involves anticipatory storage of unrequired data in buffer cache **after requested data, reducing disc access requirement**
Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: BARRETT G G; PASHA S Z; SHAHEENGOU A A; SHAHEEN-GOUDA A A
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 278471	A	19880817	EP 88101851	A	19880209	198833 B
BR 8800245	A	19880830				198839
US 4972364	A	19901120	US 89342727	A	19890424	199049
EP 278471	B1	19960117	EP 88101851	A	19880209	199608
DE 3854902	G	19960229	DE 3854902	A	19880209	199614
			EP 88101851	A	19880209	

Priority Applications (No Type Date): US 8714902 A 19870213; US 89342727 A 19890424
Cited Patents: A3...9143; EP 109309; EP 203601; EP 80875; No-SR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 278471	A	E	11		
	Designated States (Regional): DE FR GB				
EP 278471	B1	E	12	G06F-003/06	
	Designated States (Regional): DE FR GB				
DE 3854902	G			G06F-003/06	Based on patent EP 278471

Abstract (Basic): EP 278471 A

The system central processor (10) is connected by a bus (12) to an adaptor (14) serving three hard disc files (18,20,22). The storage driver software executed in the processor (30) receives commands from three command queues (32,34,36), and issues write, read, read-ahead and read- **cache** commands. A pref. 16K random-access memory **cache** (56) is

divided into 32 blocks corresp. to data retrieved from one of the discs (18,20,22) by read-ahead commands. These commands for data not requested by the processor (30) call for data stored in sequence after the data in files read in response to read commands.

ADVANTAGE - Access to rotating hard file is quickened by issue of read-ahead commands for anticipatory data transfer to adaptor **cache** , so that **disc need not** be accessed.

2/5

Title Terms: DATA; PROCESS; SYSTEM; OPERATE; ROTATING; STORAGE; ACCESS; ANTICIPATE; STORAGE; UNREQUIRED; DATA; BUFFER; **CACHE** ; AFTER; REQUEST; DATA; REDUCE; DISC; ACCESS; REQUIRE
Derwent Class: T01
International Patent Class (Main): G06F-003/06
International Patent Class (Additional): G06F-012/02; G06F-013/14
File Segment: EPI

NPL

File 2:INSPEC 1898-2006/May W1
(c) 2006 Institution of Electrical Engineers
File 6:NTIS 1964-2006/May W1
(c) 2006 NTIS, Intl Cpyrght All Rights Res
File 8:Ei Compendex(R) 1970-2006/May W1
(c) 2006 Elsevier Eng. Info. Inc.
File 23:CSA Technology Research Database 1963-2006/May
(c) 2006 CSA.
File 34:SciSearch(R) Cited Ref Sci 1990-2006/May W2
(c) 2006 Inst for Sci Info
File 35:Dissertation Abs Online 1861-2006/Apr
(c) 2006 ProQuest Info&Learning
File 65:Inside Conferences 1993-2006/May 18
(c) 2006 BLDSC all rts. reserv.
File 94:JICST-EPlus 1985-2006/Feb W2
(c)2006 Japan Science and Tech Corp(JST)
File 95:TEME-Technology & Management 1989-2006/May W2
(c) 2006 FIZ TECHNIK
File 99:Wilson Appl. Sci & Tech Abs 1983-2006/Apr
(c) 2006 The HW Wilson Co.
File 111:TGG Natl.Newspaper Index(SM) 1979-2006/May 10
(c) 2006 The Gale Group
File 144:Pascal 1973-2006/Apr W4
(c) 2006 INIST/CNRS
File 239:Mathsci 1940-2006/Jun
(c) 2006 American Mathematical Society
File 256:TecInfoSource 82-2006/Jun
(c) 2006 Info.Sources Inc
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
(c) 1998 Inst for Sci Info

Set Items Description
S1 469188 CPU OR CENTRAL()PROCESS???()UNIT? ? OR PROCESSOR? ?
S2 53838 CACHE? ?
S3 3015 TEMPORARY(3N)(STORAGE OR MEMORY)
S4 752463 EXTERNAL(3N)(STORAGE OR MEMORY) OR DISK? ? OR DISC? ? OR H-
ARD(2N)DRIVE? ? OR HARDDRIVE? ? OR HARDDISK? ? OR HARDDISC? ?
OR HDD OR HD OR RAM OR RANDOM()ACCESS()MEMORY
S5 109 S4(3N)(INACCESSIBLE OR (NO OR .NOT. OR DOESNT OR DOESN()T -
OR DONT OR DON()T OR WONT OR WON()T OR CANT OR CAN()T OR CANN-
OT OR INHIBIT??? OR PROHIBIT??? OR STOP? ? OR STOPP???)(2N)(A-
CCESS??? OR READ??? OR WRIT???))
S6 61543 POWER???(3N)(OFF OR DOWN OR STOP? ? OR STOPP??? OR (SHUT? ?
OR SHUTTING OR TURN??? OR CUT OR CUTS OR CUTTING)(3N)(OFF OR
DOWN) OR CONSERV???) OR STANDBY OR STAND()BY
S7 0 S1 AND S2:S3 AND S5 AND S6
S8 0 S1 AND S2:S3 AND S5
S9 105 S1 AND S2:S3 AND S6
S10 11 S9 AND S4
S11 9 RD (unique items)
S12 6 S11 NOT PY=2004:2006
S13 606 S4(3N)(DONT OR DON()T OR DOESNT OR DOESN()T OR "NOT" OR IS-
NT OR ISN()T)(2N)(NEED??? OR USE OR USES OR USED OR USING)
S14 20 S13 AND S2:S3
S15 10 RD (unique items)
S16 10 S15 NOT PY=2004:2006
S17 213 S2:S3 AND S6
S18 31 S17 AND S4
S19 28 RD (unique items)
S20 19 S19 NOT (S11 OR S15)
S21 14 S20 NOT PY=2004:2006
S22 68 S2:S3(5N)POWER(3N)(CONTROL? ? OR CONTROLL???)
S23 0 S22 AND S5
S24 9 S22 AND S4
S25 5 RD (unique items)
S26 3 S25 NOT PY=2004:2006
? logoff hold
18may06 10:45:29 User259273 Session D470.10

21/5/5 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06738116 E.I. No: EIP04098039963
Title: Conserving Disk Energy in Network Servers
Author: Carrera, Enrique V.; Pinheiro, Eduardo; Bianchini, Ricardo
Corporate Source: Department of Computer Science Rutgers University, Piscataway, NJ 08854-8019, United States
Conference Title: 2003 International Conference on Supercomputing
Conference Location: San Francisco, CA, United States Conference Date: 20030623-20030626
Sponsor: ACM/SIGARCH; Intel Corporation; Florida State University
E.I. Conference No.: 62275
Source: Proceedings of the International Conference on Supercomputing 2003. p 86-97

Publication Year: 2003
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 0403W2
Abstract: In this paper we study four approaches to conserving **disk** energy in high-performance network servers. The first approach is to leverage the extensive work on laptop **disks** and **power disks down** during periods of idleness. The second approach is to replace high-performance **disks** with a set of lower power **disks** that can achieve the same performance and reliability. The third approach is to combine high-performance and laptop **disks**, such that only one of these two sets of **disks** is powered on at a time. This approach requires the mirroring (and coherence) of all **disk** data on the two sets of **disks**. Finally, the fourth approach is to use multi-speed **disks**, such that each **disk** is slowed down for lower energy consumption during periods of light load. We demonstrate that the fourth approach is the only one that can actually provide energy savings for network servers. In fact, our results for Web and proxy servers show that the fourth approach can provide energy savings of up to 23%, in comparison to conventional servers, without any degradation in server performance. 31 Refs.
Descriptors: *Servers; Magnetic **disk** storage; Energy conservation; Energy utilization; Input output programs; World Wide Web; Laptop computers ; **Cache** memory; Microprocessor chips
Identifiers: Network servers; **Disk** power
Classification Codes:
722.1 (Data Storage, Equipment & Techniques); 525.2 (Energy Conservation); 525.3 (Energy Utilization); 723.1 (Computer Programming); 722.4 (Digital Computers & Systems)
722 (Computer Hardware); 723 (Computer Software, Data Handling & Applications); 525 (Energy Management); 716 (Electronic Equipment, Radar, Radio & Television); 721 (Computer Circuits & Logic Elements)
72 (COMPUTERS & DATA PROCESSING); 52 (FUEL TECHNOLOGY); 71 (ELECTRONICS & COMMUNICATION ENGINEERING)

FULL-TEXT PATENTS

File 348:EUROPEAN PATENTS 1978-2006/ 200619
(c) 2006 European Patent Office
File 349:PCT FULLTEXT 1979-2006/UB=20060511,UT=20060504
(c) 2006 WIPO/Univentio

Set	Items	Description
S1	256507	CPU OR CENTRAL()PROCESS???()UNIT? ? OR PROCESSOR? ?
S2	34994	CACHE? ?
S3	14437	TEMPORARY(3N)(STORAGE OR MEMORY)
S4	383289	EXTERNAL(3N)(STORAGE OR MEMORY) OR DISK? ? OR DISC? ? OR H-ARD(2N)DRIVE? ? OR HARDDRIVE? ? OR HARDDISK? ? OR HARDDISC? ? OR HDD OR HD OR RAM OR RANDOM()ACCESS()MEMORY

S5 1334 S4(3N)(INACCESSIBLE OR (NO OR .NOT. OR DOESNT OR DOESN()T - OR DONT OR DON()T OR WONT OR WON()T OR CANT OR CAN()T OR CANN-OT OR INHIBIT??? OR PROHIBIT??? OR STOP? ? OR STOPP???)(2N)(A-CCESS??? OR READ??? OR WRIT???))
S6 66080 POWER???(3N)(OFF OR DOWN OR STOP? ? OR STOPP??? OR (SHUT? ? OR SHUTTING OR TURN??? OR CUT OR CUTS OR CUTTING)(3N)(OFF OR DOWN) OR CONSERV???) OR STANDBY OR STAND()BY
S7 12 S2:S3(100N)S5(100N)S6
S8 12 S7 NOT AD=20031121:20060518/PR
S9 56 S2:S3(50N)S5
S10 46 S9 NOT S8
S11 44 S10 NOT AD=20031121:20060518/PR
S12 34 S11 AND IC=G06F
S13 21 S12 AND (POWER??? OR STANDBY OR STAND()BY OR SLEEP)
? logoff hold
18may06 10:57:23 User259273 Session D470.12

13/3,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01654670
Reducing TAG-RAM accesses and accelerating cache operation during cache miss
Verminderung der Zugangsgesuche eines TAG-RAM Speichers und Erhohung der Cachespeichergeschwindigkeit wahrend eines Cache-Fehltreffers
Diminution des acces a une memoire TAG-RAM et acceleration du fonctionnement d'une antememoire en cas de ratage
PATENT ASSIGNEE:
Texas Instruments Incorporated, (279078), 7839 Churchill Way, Mail Station 3999, Dallas, Texas 75251, (US), (Applicant designated States: all)
INVENTOR:
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LEGAL REPRESENTATIVE:
Holt, Michael et al (50423), Texas Instruments Limited, European Patents Department (MS 13), PO Box 5069, Northampton NN4 7ZE, (GB)
PATENT (CC, No, Kind, Date): EP 1361518 A1 031112 (Basic)
APPLICATION (CC, No, Date): EP 2003101290 030509;
PRIORITY (CC, No, Date): US 379503 P 020510
DESIGNATED STATES: DE; FR; GB
EXTENDED DESIGNATED STATES: AL; LT; LV; MK
INTERNATIONAL PATENT CLASS (V7): **G06F-012/08**
ABSTRACT WORD COUNT: 77
NOTE:
Figure number on first page: 4

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS A (English) 200346 459
SPEC A (English) 200346 5146

Total word count - document A 5605
Total word count - document B 0
Total word count - documents A + B 5605

INTERNATIONAL PATENT CLASS (V7): **G06F-012/08**

...SPECIFICATION necessary to retrieve data from a cache, the tag-RAM access is not entirely unavoidable. **Power** can be saved if it is possible to avoid access to tag-RAM. The task...

...access for retrieving data of FD2, FD3 and FD4 can be eliminated. Therefore reducing the **power** consumed by the data-RAM.

SUMMARY OF THE INVENTION
This invention is a cache memory...

...is absolutely necessary, the tag-RAM access is not entirely unavoidable. It is preferred from **power** saving point of view not to access tag-RAM if possible. This required determining under...

...cache system with four entries per cache line. As a result, the tag-RAM access **power** can be reduced by a factor of four. In addition, the present invention improves the...

...CLAIMS last hit-line address and providing a match indication or a non-match indication;
a **cache** data-RAM storing data and corresponding memory addresses;
a tag-RAM storing indications of addresses of data stored in **cache** data-RAM;
a tag-RAM controller connected to said **cache** line comparator and said tag-RAM, said tag- **RAM** controller operative to
prohibit access to said tag- **RAM** to determine if data corresponding to said current memory access request address is stored in said **cache** data-RAM if said **cache** line comparator provides said match indication, and
enable access to said tag-RAM to determine...

13/3,K/6 (Item 6 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01262240
Portable information processing terminal device with low power **consumption and large memory capacity**
Tragbares Informationsverarbeitungsendgerat mit geringem Leistungsverbrauch und grosser Speicherkapazitat
Appareil terminal portatif de traitement d'informations a faible consommation d'energie et grande capacite de memoire
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PATENT (CC, No, Kind, Date): EP 1089159 A2 010404 (Basic)
EP 1089159 A3 031022
APPLICATION (CC, No, Date): EP 2000307881 000912;
PRIORITY (CC, No, Date): JP 99278260 990930
DESIGNATED STATES: DE; FR; GB
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS (V7): **G06F-001/32**
ABSTRACT WORD COUNT: 172
NOTE:
Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS A (English) 200114 978
SPEC A (English) 200114 11230
Total word count - document A 12208
Total word count - document B 0
Total word count - documents A + B 12208

Portable information processing terminal device with low power **consumption and large memory capacity**

INTERNATIONAL PATENT CLASS (V7): **G06F-001/32**

...ABSTRACT A2

A portable information processing terminal device, realizing both a low **power** consumption and a large memory capacity, is formed by a first memory for storing files...

...a plurality of files, the second memory having a larger memory capacity and a higher **power** consumption than the first memory, a processing unit configured to read and process files stored...

<File reading/writing processing>

In the...

...point, upon receiving the file reading request, the file management unit 102 searches through the **cache** 17 by referring to the **cache** management table first, and when this file is in the **cache** 17 this file is read out from the **cache** 17 (steps S11, S12).

Then, the file management unit 102 judges whether it is in the disk access permitted state or the **disk access prohibited** state (step S13). When activation of the disk device 16 is not prohibited by the...

...disk access permitted state, the file management unit 102 checks the update information of the **cache** management table, and judges whether the reading requested file in the cache 17 is updated...

...unit 102 updates relevant fields (storing location, update information, last access time, etc.) of the **cache** management table according to the need (step S16).

In the case where the reading requested file cannot be found in the **cache** 17 (step S11 NO), the file management unit 102 judges whether it

is in the disk access permitted state or the **disk access prohibited** state (step S17). When activation of the disk device 16 is not prohibited by the...

...disk device 16 is checked, and a copy of the file is created in the **cache** 17 only when this file is a file which has a high probability of being accessed during a period of the **disk access prohibited** state such as a period of the battery driven mode. In addition, even in the...

...unit 102 updates relevant fields (storing location, update information, last access time, etc.) of the **cache** management table according to the need (step S16), and the processing is terminated.

Note that, even in the case where the **disk access** is **prohibited**, if the **reading** request file exists only on the disk device 16, it is possible to permit the disk access by temporarily judging that there is a possibility of external **power** supply. The exemplary processing procedure in this case is shown in Fig. 5.

In Fig...